REMARKS

I. Amendments to the Drawings

The drawings were objected to because Figures 8-10 were too dark after scanning. In response to this objection, Applicants submit herewith replacement sheets that contain the appropriate corrections.

II. Objection to Claim 2

Claim 2 was objected to because it was believed that (c) and (d) should be changed to (a) and (b), respectively. Applicants respectfully disagree. Claim 1 already recites (a) and (b), and Claim 2 depends from Claim 1. If (c) and (d) in Claim 2 were changed to (a) and (b), there would be two (a)'s and two (b)'s — one set from Claim 1 and another set from dependent Claim 2. Accordingly, Applicants respectfully submit that no correction is needed and request that the objection to Claim 2 be removed.

III. 35 U.S.C. § 112, Second Paragraph, Rejections

Claims 2, 22, 38, and 44 were rejected under 35 U.S.C. § 112, second paragraph. It was asserted that the phase "in response to reading the flag stored in the set of memory cells, reading the redundant block" is indefinite because it does not distinctly point out which set of memory the flag is read from (i.e., the primary block or the redundant block). In response to this rejection, Applicants have amended Claims 2, 22, 38, and 44 to include the phrase "allocated to the primary block." In view of these amendments, Applicants respectfully submit that the 35 U.S.C. § 112, second paragraph, rejections have been overcome.

IV. 35 U.S.C. § 102(b) Rejections

Independent Claims 1, 18, and 44 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,831,989 to Fukisaki. Applicants respectfully request

reconsideration and withdrawal of these rejections because Fukisaki does not teach each and every element in the independent claims.

A. Independent Claims 1 and 44

Independent Claims 1 and 44 recite a memory array comprising a primary block of memory cells and the act of storing a flag in a set of memory cells allocated to the primary block in response to an error in writing to the primary block. To clarify the claims and make explicit what is implicit, Applicants have amended Claims 1 and 44 to recite that the set of memory cells in which the flag is stored is ***in the memory array***. This is not shown in Fujisaki.

Fujisaki is directed to a testing apparatus for a memory array (the "memory under test (MUT)"). As noted in the Office Action, Figure 6 shows that the MUT has a main memory cell array (the purported primary block) and row and column address relief lines (the purported redundant block). As shown in Figure 5, the testing apparatus is "built around" the MUT and contains a failure analysis memory 5 that is separate from the MUT. As also noted in the Office Action, col. 2, lines 10-23 of Fujisaki teach writing a logical 1 (the purported flag) in the failure analysis memory 5 when the testing apparatus finds a failure in the MUT. In operation, the testing apparatus writes a test pattern to the main memory array of the MUT and determines whether the test pattern was written correctly. If the test pattern was not written correctly, a logical 1 is written in the failure analysis memory 5. As is clearly shown in Figure 5 and described in Fujisaki, the ***failure analysis memory 5 is not part of the MUT***. Accordingly, the purported flag in Fujisaki is not stored in the same memory array that contains the primary block. In contrast, Claims 1 and 44 require the flag to be stored ***in the memory array that contains the primary block***.

This highlights the difference between Fujisaki and at least some of Applicants' preferred embodiments. In Fujisaki, the "flag" is stored in the failure analysis memory 5 to count the number of failed memory cells to determine whether or not there is a sufficient number of extra rows and columns in the memory array to handle the failures. As such, the flag is stored in the testing apparatus and not in the memory array being tested. In contrast, in Claim 44, the recited flag written in the memory array is accessed during a subsequent write operation to the memory array to determine that the data should be written in the redundant block instead of the primary block.

In summary, because Fujisaki does not store its flag in the memory array that contains the primary and redundant memory arrays, Applicants respectfully submit that Fujisaki fails to anticipate independent Claims 1 and 44 and, therefore, the rejections of those claims should be removed.

B. Independent Claim 18

Pages 8-9 of Applicants' specification described two approaches to determining whether an error occurred in writing to memory. In the first approach, data is written to memory, a separate read operation is used to read the stored data out of the memory, and the read data is compared with the data expected to be stored in the memory. In the second approach, instead of writing, reading, and then comparing, an error is determined while attempting to write to the memory. The second approach avoids the overhead associated with the first approach of switching from a write voltage condition to a read voltage condition to determine whether an error occurred.

Independent Claim 18 is directed to the second approach, while Fujisaki uses the first approach. Independent Claim 18 recites ***while attempting to write to the primary block,***

determining that an error occurred in writing to the primary block. In contrast, as described at col. 1, lines 54-55, Fujisaki teaches the write-read-compare approach:

> The data signal written in the memory under test MUT is temporarily stored therein and ***is read out therefrom later***. ***The read-out data signal*** is inputted to the logical comparator 4. An expected value data signal is supplied from the pattern generator 2 to the logical comparator 4 where the data signal inputted thereto from the memory under test MUT is ***logically compared*** with the expected value data signal to detect as to whether or not there is an anti-coincidence or mismatch between both signal. (Emphasis added)

In summary, Fujisaki teaches the write-read-compare approach to determine an error — not the while-attempting-to-write approach as recited in independent Claim 18. Accordingly, Applicants respectfully submit that Fujisaki fails to anticipate independent Claim 18 and, therefore, that the rejection against independent Claim 18 should be removed.

V. 35 U.S.C. § 103(a) Rejection of Independent Claim 36

Independent Claim 36 recites "a three-dimensional memory array of vertically-stacked field-programmable memory cells" and was rejected under 35 U.S.C. § 103(a) as being unpatentable over the proposed combination of Fukisaki and U.S. Patent No. 5,278,839 to Matsumoto et al. In the Office Action, it was admitted that Fukisaki fails to disclose the recited three-dimensional memory array, and Matsumoto et al. was relied upon to cure the deficiency. However, like Fukisaki, Matsumoto et al. fails to teach a three-dimensional memory array of vertically-stacked field-programmable memory cells.

Matsumoto et al. discloses a memory cell array and a redundant memory cell array. Col. 3, lines 31-35 and 42-45 teach that these arrays comprises memory cells that are "arranged in the shape of a matrix." There is no teaching whatsoever in Matsumoto et al. that the memory cells are arranged in a vertical stack to form a three-dimensional memory array, as recited in independent Claim 36. Further, it was noted in the Office Action that col. 9, lines 4-39 of

Matsumoto et al. teaches that the memory cells in the memory arrays are bipolar PROM transistors. However, this disclosure merely describes the type of memory cell that is used and does not teach that the memory cells are vertically stacked to form a three-dimensional array, as recited in independent Claim 36.

In summary, because neither Fukisaki nor Matsumoto et al. teaches a three-dimensional memory array of vertically-stacked field-programmable memory cells, the proposed combination of Fukisaki and Matsumoto et al. necessarily fails render independent Claim 36 unpatentable. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection of independent Claim 36.

VI. The Dependent Claims Are Patentable over the Cited References

Because the independent claims are patentable over the cited references, the dependent claims are necessarily also patentable over the cited references. Applicants note that the dependent claims recite additional features that provide additional grounds of patentability over the cited references. Applicants reserve the right to present arguments concerning these additional grounds at a later time, if necessary.

VII. Conclusion

In view of the above amendments and remarks, Applicants respectfully submit that this application is in condition for allowance. Reconsideration is respectfully requested. If there are any questions concerning this Amendment, the Examiner is invited to contact the undersigned attorney at (312) 321-4719.

Dated: October 19, 2004

Respectfully submitted,

Joseph F. Hetz
Reg. No. 41,070
Attorney for Applicants

BRINKS HOFER
GILSON & LIONE
P.O. Box 10395
Chicago, Illinois 60610
(312) 321-4719